** 2022-2023**

**Sessional Test I–March, 2023**

**SET-D Solution**

Roll No: ………………

Programme: B.E. Time: 90 minutes

Course Title: Computer Organization and Architecture

Course Code: CS157 Max. Marks: 40

General Instructions:

* Follow the instructions given in each section.
* Do not write anything on the question paper, except your roll no.
* Make sure that you attempt the questions in order.

Section - A

(Q 1 to 5: Each question carries 1 mark)

Q1.   In a 4-bit ripple counter, how many natural states will be there?

**Ans. (c) 16 states.**

Q2. Computer has to perform a particular operation in which of the following is a group of bits that tells the computer to do?

**Ans. (c) Instruction Code**

Q3. The Boolean expression for a 3-input AND gate is \_\_\_\_\_\_\_\_.

**Ans. (b) X = ABC**

Q4. The output of an EX-NOR gate is 1. Which input combination is correct?

**Ans. (c) A = 0, B = 0**

Q5. The most common addressing techniques employed by a CPU is:

1. Direct
2. Indirect
3. Immediate
4. All of these

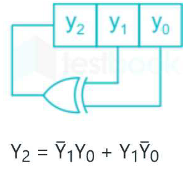
**Ans. (d) All of these**

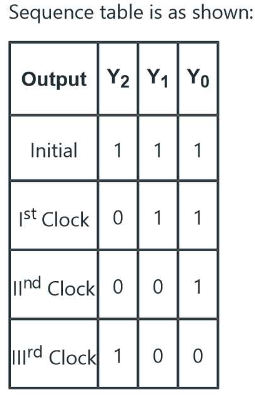
Section - B

(Q 6 to 10: Each question carries 3 marks)

Q6. A three-bit pseudo random number generator is shown in Fig 1. Initially the value of Y2Y1Y0 is set to 111. The value of output *Y* after three clock cycles is.

**Ans.-** Given sequential circuit can be redrawn as:





So, after 3rd clock cycles, value of the output would be 100.

Q7. What will be the output of the given logic gate circuit is given in Fig.2 ? Write the expression after each gate for input A, B, C, D.

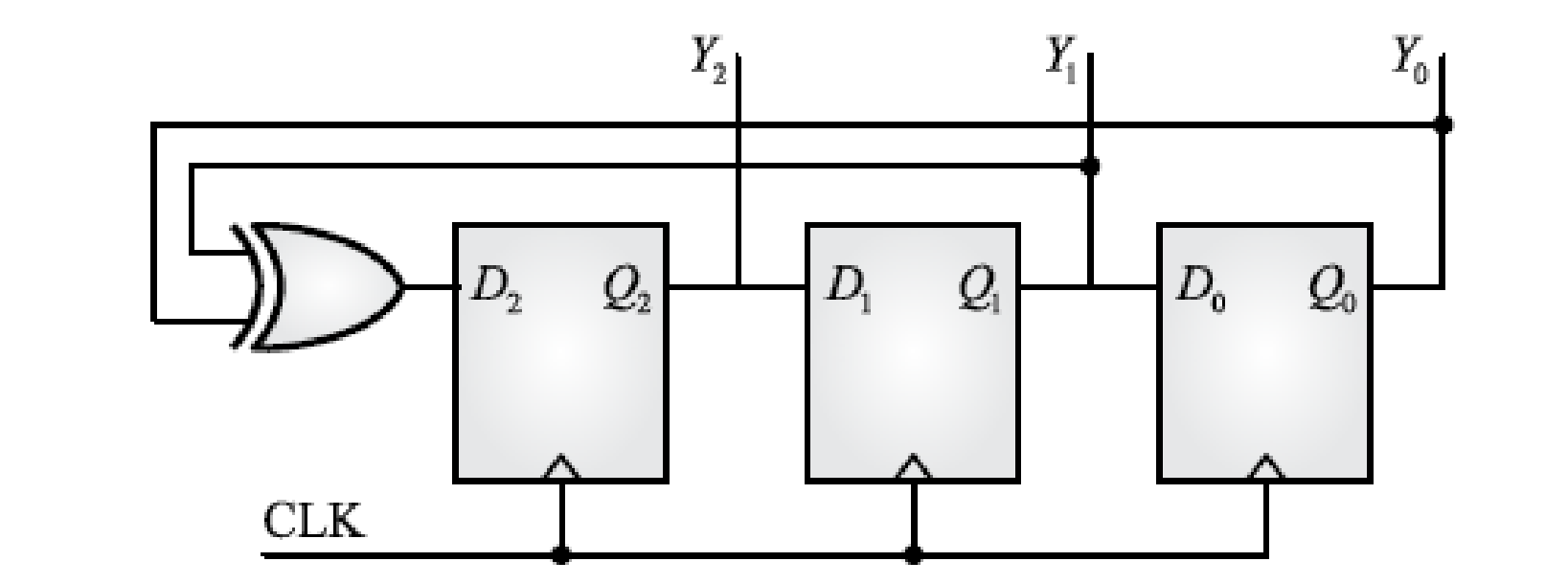
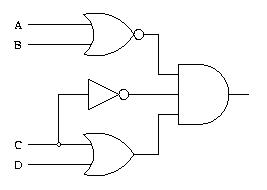
 

Fig1 Fig2

**Ans.** Output after NOR gate= (A+B)’

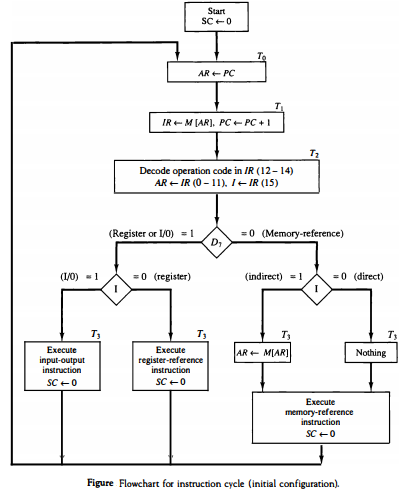
Output after OR gate= C+D

Output after NOT gate= C’

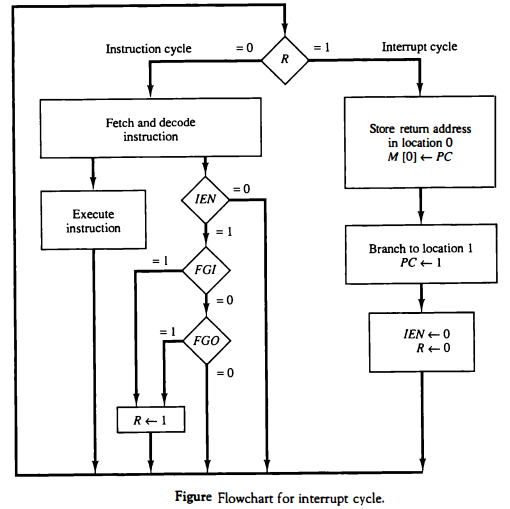
Final output after AND gate= (A+B)’.C’. (C+D)

Q8. To determine the type of instruction, make a flow chart depicting the complete instruction cycle.

**Ans**. To determine the type of instruction, following flow chart has to follow:



Q9. How does computer handle the program interrupt. Explain using flow chart for the same.

**Ans**. 

Q10. A computer uses a memory unit with 256k words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers and an address part.

1. How many bits are there in the operation code, the register part and the address part?
2. Draw an instruction word format and indicate the number of bits in each part.

**Ans.**

1 word=32 bits=4 bytes

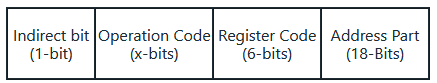
Memory Size= 256K words= 218 words

Number of registers=n=64

Indirect bit=1

Number of bits required to present a register= 64=2n=6 bits

Binary instruction= 32 bits



1+x+6+18=32

x=7 bits

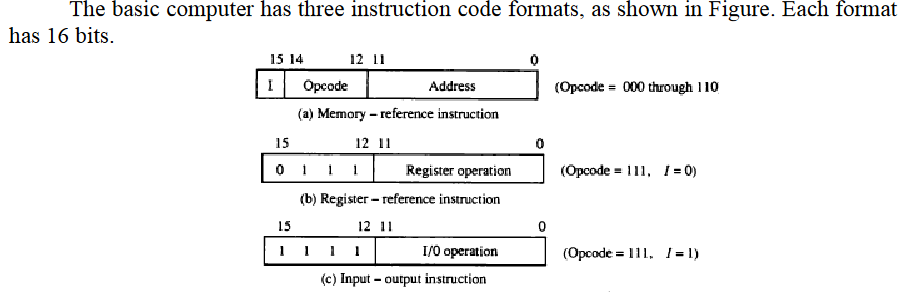
Therefore 7, 6 and 18 bits are required in operation code, the register code part, and address part respectively.

Section – C

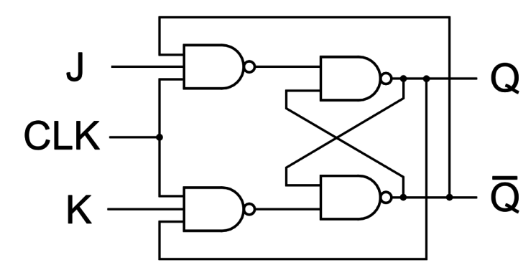
(Q 11 to 12: Each question carries 5 marks)

Q11. For the memory 4096\*16, illustrate the basic computer instruction formats.

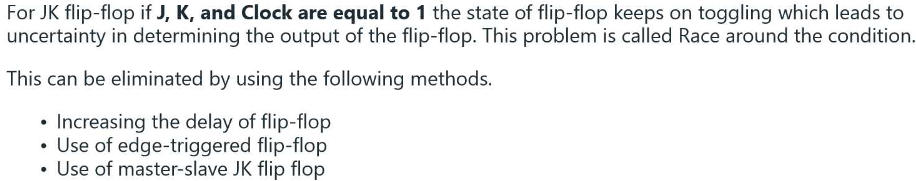
**Ans.**

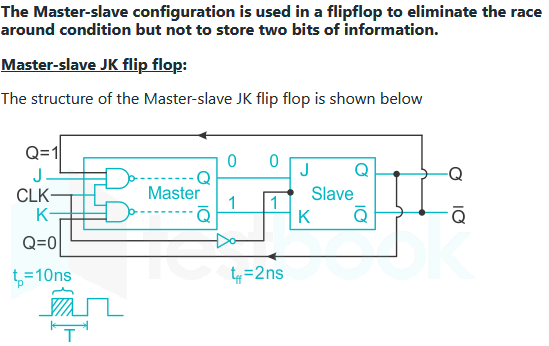


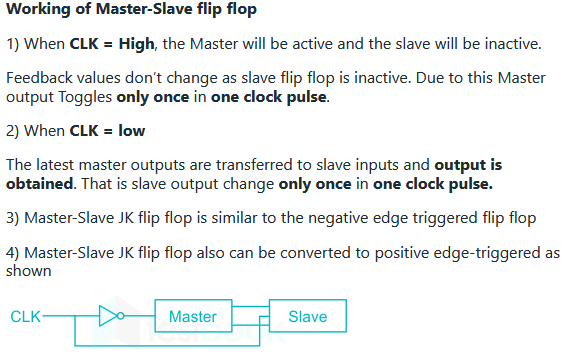
Q12. As shown in circuit below, when J=K=1, CLK = 1, how do you define this condition in JK flipflop and what are the solutions to remove this condition.



**Ans.**







Section – D

(Q 13: Question carries 10 marks)

Q13. a) An instruction at address 021 in the basic computer has an address part equal to 083 (all numbers are in hexadecimal). The memory word at address 083 contains the operand C5F6 and the content of AC (Accumulator) is B947. Determine the contents of the registers at the end of the execute phase: PC (Program Counter), AR (Address Register), AC and IR (Instruction Register). Implement the problem using following operation codes (Hexadecimal code):

i) ADD (1083)

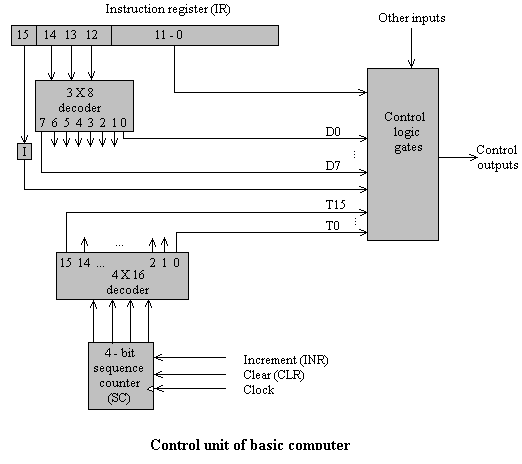
ii) BUN (4083)

**Ans.**

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| Instruction | PC | AR | DR | AC | IR |
| Initial | 021 | - | - | B567 | - |
| ADD(1083) | 022 | 083 | C5F6 | 7F3D | 1083 |
| BUN (4083) | 083 | 083 | -- | B567 | 4083 |

b) To select the timing signal and opcode using decoder draw the control unit of basic computer. (6+4 = 10)

**Ans.**



The instruction register is divided into three parts:

1. the 1 bit,
2. the operation code, and
3. bits 0 through 11.
4. The operation code in bits 12 through 14 are decoded with a 3 x 8 decoder. The eight outputs of the decoder are designated by the symbols D0 through D7. The subscripted decimal number is equivalent to the binary value of the corresponding operation code. Bit 15 of the instruction is transferred to a flip-flop designated by the symbol I. Bits 0 through 11 are applied to the control logic gates. The 4-bit sequence counter can count in binary from 0 through 15. The outputs of the counter are decoded into 16 timing signals T0 through T15.
5. The sequence counter SC can be incremented or cleared synchronously. Most of the time, the counter is incremented to provide the sequence of timing signals out of the 4 x 16 decoder. Once in a while, the counter is cleared to 0, causing the next active timing signal to be T0.
6. As an example, consider the case where SC is incremented to provide timing signals T0, T1, T2, T3, and T4 in sequence. At time T4, SC is cleared to 0 if decoder output D3 is active. This is expressed symbolically by the statement

D3T4: SC <\_\_ 0